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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Hagh-Panah et al.

Serial No. 10/068,676

Filed: February 4, 2002

For: PARALLEL CRC FORMULATION

§ Group Art Unit: 2133
§ Examiner: Joseph D. Torres
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§ Atty. Dkt. No. 5298-10900
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October 12, 2005
Date

Ann Marie Mewherter

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Sir/Madam:

Further to the Notice of Appeal faxed on August 12, 2005, the Appellant presents this Appeal Brief. The Notice of Appeal was filed following receipt of an Advisory Action mailed August 9, 2005. The Appellant hereby appeals to the Board of Patent Appeals and Interferences the final rejection of claims 1-5 and 11-20 and respectfully requests that this appeal be considered by the Board.

I. REAL PARTY IN INTEREST

The subject application is owned by Cypress Semiconductor Corporation, a corporation having its principal place of business at 3901 North First Street, San Jose, California, 95134, as evidenced by the assignment recorded at Reel 012576, Frame 0581.

II. RELATED APPEALS AND INTERFERENCES

No other prior and pending appeals, interferences, or judicial proceedings are known to Appellant or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-5 and 11-20 stand finally rejected. Claims 6-10 were withdrawn from consideration in response to the Election/Restriction requirement mailed June 21, 2004. No claims have been allowed, objected to or canceled. Claims 1-5 and 11-20 are being appealed.

IV. STATUS OF AMENDMENTS

No amendments to the claims have been filed subsequent to their final rejection. The Claims Appendix attached hereto reflects the current state of the claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellant's claimed subject matter includes a method of performing a cyclic redundancy check (CRC) calculation on a data stream composed of one or more segments of data. In general, CRC circuits used to implement the method may perform a mathematical calculation on the data stream before and after data transmission. If the two results are identical, then it is assumed that no errors occurred during transmission. (*See*, e.g., Specification – paragraph 0008, page 3; FIG. 7A).

According to one embodiment, the presently claimed method may include the step of supplying the data stream, one data segment per cycle, to a multiple-byte cyclic redundancy check (CRC) circuit comprising a plurality of CRC modules. In some cases, the multiple-byte CRC circuit may include a first CRC module, a second CRC module and a decision module (*See*, e.g., Specification – paragraph 0026, page 10). In other cases, the multiple-byte CRC circuit may include a total of eight CRC modules, for example (*See*, e.g., Specification – paragraph 0028, page 10). Regardless, each of the CRC modules may be configured to perform the CRC calculation on a different number of bytes of data during a single cycle. For example, if a total of eight CRC modules are used, an eight-byte-wide CRC module may be

included for performing a CRC calculation on an eight-byte-wide segment of data, a seven-byte-wide CRC module may be included for performing a CRC calculation on a seven-byte-wide segment of data, etc. (*See*, e.g., Specification – paragraph 0027, page 10; and paragraph 0049, pages 15-16).

In addition, the presently claimed method may include the step of determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit. In some cases, the decision module may direct the segment of data to one of the eight CRC modules, depending on the number of bytes of data to be processed. For example, a single-byte CRC module would be used if the segment of data includes only one byte. If there are two bytes remaining, a two-byte CRC module would be used, etc. (*See*, e.g., Specification – paragraph 0028, page 10; paragraph 0029, pages 10-11; paragraph 0050, page 16; paragraph 0054, page 17).

After the step of determining, the method may include processing the segment of data using only the CRC module determined appropriate for the current segment of data (which is based on the number of bytes of data to be processed). As noted in the presently claimed case, the step of processing includes performing the CRC calculation (i.e., performing a mathematical cyclic redundancy check calculation) on the current segment of data to produce CRC calculation results for the current cycle. If more segments of data remain in the data stream, the steps of determining and processing are repeated until there are no more segments of data to process. (Specification – paragraph 0051-0053, pages 16-17).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3-5 and 11-20 are rejected under 35 U.S.C § 102(c) as being anticipated by U.S. Patent No. 6,530,057 to Kimmitt (hereinafter referred to as "Kimmitt").

2. Claim 2 is rejected under 35 U.S.C § 103(a) as being unpatentable over Kimmitt in view of U.S. Patent No. 5,050,165 to Yoshioka et al. (hereinafter referred to as "Yoshioka").

VII. ARGUMENT

The contentions of the Appellant with respect to the ground of rejection presented for review, and the basis thereof, with citations of the statutes, regulations, authorities, and parts of the record relied on are presented herein for consideration by the Board.

A. Patentability of Claims 1, 3-5 and 11-20:

Claims 1, 3-5, and 11-20 were rejected under 35 U.S.C. §102(e) as being anticipated by Kimmitt. The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. More specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d. 1382 (CCPA 1970). Kimmitt does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

1. **Kimmitt fails to anticipate a method for performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes: (i) determining which one of a plurality of CRC modules – each configured to perform the CRC calculation on a different number of bytes of data – should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and (ii) after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data.**

Independent claim 1 recites, in part:

> A method of performing a cyclic redundancy check (CRC) calculation on a data stream composed of one or more segments of data, the method comprising: supplying the data stream, one data segment per cycle, to a multiple-byte cyclic redundancy check (CRC) circuit comprising a plurality of CRC modules, wherein each of the CRC modules is configured to perform the CRC calculation on a different number of bytes of data during a single cycle; determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit; after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data, wherein said step of processing comprises performing the CRC calculation on the current segment of data to produce CRC calculation results for the current cycle...

Statements in the Final Office Action suggest that Kimmitt provides teaching for all limitations of present claim 1, and more specifically, that teaching for the present limitations may be found in columns 14-15 and Fig. 7 of Kimmitt (*See*, Final Office Action, pages 3-4). The Applicant disagrees. As set forth in more detail below, Kimmitt fails to anticipate all limitations of present claim 1. As such, Applicants contend that the §102 rejection of present claim 1, and all claims dependent therefrom, cannot be maintained.

In columns 14-15, Kimmitt discloses a 32-bit wide CRC generator-checker including "CRC logic modules 100, remainder registers 102, input data register 104, CRC Controller State Machine 106, multiplexer 108, and inverter [110]." (Kimmitt, column 14, lines 35-43; Fig. 7). Kimmitt further teaches that, during operation of the embodiment shown in Fig. 7, "input data 50 is received into the input register 104, and subsequently input to the CRC logic modules 100. The input data is passed to the CRC logic modules 100 in 32 bit portions ... [t]he outputs of the CRC modules 100 are then stored in the remainder registers 102, and fed back as r31 ... r0 135 into the CRC logic modules 100. This process repeats recursively until all the input data 50 has been processed." (Kimmitt, column 14, lines 45-54).

As such, Kimmitt appears to disclose a method in which an input data stream (50) is supplied to a CRC circuit having a plurality of CRC modules (100a-100d), each configured for processing 32 bits of data (r31 ... r0) at a time. In the method disclosed by Kimmitt, each one of the CRC modules processes 32 bits of data, and outputs a CRC result to a corresponding 32 bit remainder register (102a-102d). Kimmitt further teaches that, "[a]t the end of the input data 50, the multiplexer 108 outputs the final contents of a selected one of the 32-bit remainder registers 102, based on the assertion of its controls 112." (Kimmitt, column 14, lines 54-59).

As pointed out by the Examiner, Kimmitt also proposes a method for handling termination sequences (i.e., the last data segment in a data stream) with less than 32 valid bits. For example, Kimmitt discloses that, "logic blocks 100a, 100b and 100c are termination logic blocks for handling termination sequences having 24, 16 and 8 valid bits respectively." (Kimmitt, column 15, lines 18-20; Fig. 7). Kimmitt also discloses that, when the last word of a message is detected (e.g., by assertion of last word signal 109):

> CRC controller state machine [106] detects the number of valid bytes in the last word from valid bytes signal 107. The CRC controller state machine 106 also appends n zero bits at the end of the message... by selecting the hardwired zero input 111 of the multiplexer 104 when the final byte of the last word of the message has been received. The CRC controller state machine 106 then selects which remainder register of

> remainder registers 102 holds the last value to be passed through the multiplexer 108. Specifically... if there are 8 valid bits in the final word, the CRC controller state machine operates to select the remainder register 102a using the controls 112 of the multiplexer 108... if there are 16 valid bits the contents of remainder register 102b is selected... [etc.]" (Kimmitt, column 15, lines 24-32).

As such, the method of Kimmitt handles termination sequences by padding the last word of the message with zeros (if the number of valid bytes in the last word is less than the standard 32 bits), supplying the (zero padded) last word to all CRC modules 100a-100d, and selecting the appropriate CRC result from one of the remainder registers 102a-102d, depending on the number of valid bytes in the last word.

On page 3 of the Final Office Action, the Examiner alleges that CRC controller state machine 106 is used "for determining which one of the CRC modules 100a to 100d should be used for processing the segment of data currently supplied to the Multi-byte CRC circuit." More specifically, the Examiner suggests that "CRC Controller State Machine 106 processes data in 4-byte data segments until the last segment of data is reached whereby CRC Controller State Machine 106 uses the size of the last segment to determine which CRC module will be used" (Final Office Action, page 3). The Applicant disagrees. As set forth below, CRC controller state machine 106 is not used for determining which one of the plurality of CRC modules should be used for processing the segment of data.

Contrary to the presently claimed case, the CRC controller state machine of Kimmitt does not determine which one of the plurality of CRC modules (e.g., 100a-100d in FIG. 7) to use before the last word is processed. Instead, Kimmitt explicitly teaches that the last word is processed by all CRC modules, the results of which are stored within remainder registers 102a-102d. The CRC controller state machine 106 is then used to select which remainder register of remainder registers 102 holds the last value to be passed through the multiplexer 108. (*See*, Kimmitt, column 15, lines 18-44). In this manner, CRC controller state machine 106 fails to determine which one of the CRC modules should be used for processing the final bits of the last word before the final word is processed.

On page 2 of the Advisory Action, the Examiner suggests that CRC controller state machine 106 and multiplexer 108 of Kimmitt provide teaching for the presently claimed steps of determining and processing, respectively. For example, the Examiner suggests that "column 15, lines 33-35 in Kimmitt teach that the CRC controller state machine 106 selects which remainder register of remainder registers 102 holds the last value to be processed through the multiplexer 108. In addition, column 14, lines 62-65 in Kimmitt teach that selection of the correct CRC from the array of CRC remainder registers (102a-102d

in FIG. 7) is done with a multiplexer (108 in FIG. 7) in hardware; hence Kimmitt explicitly teaches CRC controller state machine 106 and Multiplexer 108 in Figure 7 of Kimmitt for determining which one of a plurality of CRC modules -- each configured to perform the CRC calculation on a different number of bytes of data -- should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data (Note: Multiplexer 108 in Figure 7 of Kimmitt processes the segment of data using only the selected CRC module determined appropriate by the CRC controller state machine 106 for the current segment of data)." The Applicant disagrees.

As noted above, CRC controller state machine 106 does not select the appropriate CRC module to be used for processing the current segment of data, but instead, selects the appropriate remainder register holding the correct CRC result. The Examiner notes this fact in the above-mentioned Advisory Action statements. However, the Examiner suggests that the "selection of the correct CRC from the array of CRC remainder registers (102a-102d in FIG. 7) is done with a multiplexer (108 in FIG. 7) in hardware" (Advisory Action, page 2). Therefore, the Examiner appears to suggest that, when combined together, the CRC controller state machine 106 and multiplexer 108 disclosed by Kimmitt provide teaching for the presently claimed steps of determining and processing. This is simply not true.

First of all, although Kimmitt discloses that multiplexer 108 may be used to select a final CRC output from one of the remainder registers (102a-102d), such selection is performed after the final data segment has been processed by each and every one of the CRC modules (100a-100d) and corresponding results have been stored within each of the remainder registers (*See*, e.g., Kimmitt, column 15, lines 33-44). Therefore, multiplexer 108 cannot be combined with CRC controller state machine 106 to determine which one of the CRC modules should be used for processing the final data segments before the final data segments are processed.

Furthermore, Kimmitt fails to disclose that multiplexer 108 can be used to "process" the current data segment, as recited in present claim 1. For instance, Kimmitt teaches that multiplexer 108 may be used for selecting a CRC result from one of the remainder registers. This is consistent with knowledge generally available to one of ordinary skill in the art (i.e., multiplexers are well-known logic selection devices). However, Kimmitt does not teach or suggest that multiplexer 108 may be used for "processing" the data segments, where the step of processing is explicitly described in the claims as "performing the CRC calculation on the current segment of data to produce CRC calculation results for the current

cycle." In fact, one skilled in the art would never conclude that a multiplexer was somehow capable of performing a CRC calculation on a segment of data. In addition, Appellants contend that multiplexer 108 is simply incapable of "processing" the data segments, as set forth in present claim 1. Therefore, multiplexer 108 cannot be relied upon to provide teaching for the presently claimed step of processing.

2. The Examiner has failed to support a ground of anticipation of present claim 1 by DiNicola.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. As pointed out above, Kimmitt does not disclose a method for performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes determining which one of a plurality of CRC modules -- each configured to perform the CRC calculation on a different number of bytes of data -- should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, as recited in present claim 1. In addition, Kimmitt does not disclose that, after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data, as further recited in present claim 1. Kimmitt, therefore, cannot teach each and every element set forth in claim 1. As a consequence, claim 1 is not anticipated by Kimmitt.

Conclusion

As explained in Arguments 1-2 above, several limitations of independent claim 1 is not taught or suggested by Kimmitt. Therefore, claim 1 is not anticipated by Kimmitt. Since claims 2-5 and 11-20 are dependent from claim 1, claims 2-5 and 11-20 are also not anticipated by Kimmitt. The rejection of claims 1, 3-5 and 11-20 under 35 U.S.C. §102 is, therefore, asserted to be erroneous.

B. Patentability of Claim 2:

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimmitt in view of Yoshioka. To establish a case of *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or

motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); MPEP 2143.01. The cited art does not teach or suggest each and every limitation of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Yoshioka cannot be combined with Kimmitt to provide teaching or suggestion for the combined limitations of present claims 1 and 2.

As noted above, independent claim 1 recites limitations on a method for performing a cyclic redundancy check (CRC) calculation on a data stream, where the method includes: (i) determining which one of a plurality of CRC modules -- each configured to perform the CRC calculation on a different number of bytes of data -- should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit, and (ii) after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data. Dependent claim 2 places an additional limitation on claim 1 by suggesting that the method may be used in an interface circuit board.

Statements in the Final Office Action suggest that while "Kimmitt substantially teaches the claimed invention described in claim 1 ... Kimmitt does not explicitly teach the specific use of an interface circuit board. Yoshioka, in an analogous art, teaches [the] use of an interface circuit board." (Final Office Action, page 11). Further statements in the final Office Action suggest that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kimmitt with the teachings of Yoshioka by including [the] use of an interface circuit board." As described in more detail below, Kimmitt and Yoshioka fail to teach or suggest all limitations of present claims 1 and 2 and, furthermore, cannot be combined or modified to do so.

As noted above in the arguments for the patentability of claims 1, 3-5 and 11-20, Kimmitt fails to disclose all limitations of present claim 1. In addition to explicit lack of teaching, Kimmitt fails to provide motivation for the aforementioned limitations. For example, Kimmitt fails to suggest a desirability for the aforementioned method steps. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination [or modification]. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01. By failing to suggest a desirability for the above-mentioned method steps,

Kimmitt provides absolutely no motivation that would enable one skilled in the art to modify the teachings of Kimmitt to include such steps.

Like Kimmitt, Yoshioka also fails to teach, suggest or provide motivation for the aforementioned method steps recited in claim 1. The Examiner admits that Yoshioka was not relied upon (and therefore does not disclose) the limitations of present claim 1 (See, e.g., Advisory Action, page 2). Therefore, even if Yoshioka were to provide teaching for incorporating a CRC circuit within an interface circuit board (as suggested in the Final Office Action), the combined teachings of Kimmitt and Yoshioka would still fail to disclose the combined limitations recited in claims 1 and 2.

Conclusion

As explained above, Kimmitt and Yoshioka each fail to teach, suggest or provide motivation for all limitations of claims 1 and 2. In addition, Kimmitt and Yoshioka cannot be combined or modified to do so. For at least these reasons, the limitations of claims 1 and 2 are considered to be patentably distinct over Kimmitt and Yoshioka. Therefore, the §103(a) rejection of claim 2 over Kimmitt and Yoshioka is asserted to be erroneous.

CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-5 and 11-20 was erroneous, and reversal of the decision is respectfully requested.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

The present claims on appeal are as follows.

1. A method of performing a cyclic redundancy check (CRC) calculation on a data stream composed of one or more segments of data, the method comprising:

supplying the data stream, one data segment per cycle, to a multiple-byte cyclic redundancy check (CRC) circuit comprising a plurality of CRC modules, wherein each of the CRC modules is configured to perform the CRC calculation on a different number of bytes of data during a single cycle;

determining which one of the plurality of CRC modules should be used for processing a segment of data currently supplied to the multiple-byte CRC circuit;

after said step of determining, processing the segment of data using only the CRC module determined appropriate for the current segment of data, wherein said step of processing comprises performing the CRC calculation on the current segment of data to produce CRC calculation results for the current cycle; and

if more segments of data remain in the data stream, repeating the steps of determining and processing until there are no more segments of data to process.

2. The method of claim 1, wherein the method of performing a cyclic redundancy check calculation on a data stream is used in an interface circuit board.

3. The method of claim 2, wherein the maximum number of bytes is eight bytes of data.

4. The method of claim 3, wherein the plurality of CRC modules includes:

an eight byte-wide CRC module configured to perform a CRC calculation on an eight-byte-wide segment of data;

a seven byte-wide CRC module configured to perform a CRC calculation on a seven-byte-wide segment of data;

a six byte-wide CRC module configured to perform a CRC calculation on a six-byte-wide segment of data;

a five byte-wide CRC module configured to perform a CRC calculation on a five-byte-wide segment of data;

a four byte-wide CRC module configured to perform a CRC calculation on a four-byte-wide segment of data;

a three byte-wide CRC module configured to perform a CRC calculation on a three-byte-wide segment of data;

a two byte-wide CRC module configured to perform a CRC calculation on a two-byte-wide segment of data; and

a single byte-wide CRC module configured to perform a CRC calculation on a one-byte-wide segment of data.

5. The method of claim 1, wherein the multiple-byte CRC circuit uses a CRC-32 generator polynomial for performing the CRC calculation.

11. The method of claim 1, wherein at least one of the plurality of CRC modules is configured to perform the CRC calculation on a minimum number of bytes during a single cycle, and wherein the minimum number of bytes is substantially equal to one.

12. The method of claim 11, wherein at least one of the plurality of CRC modules is configured to perform the CRC calculation on a maximum number of bytes during a single cycle, and wherein the maximum number of bytes is selected from a range of integer values encompassing eight.

13. The method of claim 12, wherein each of the plurality of CRC modules is configured for using prior CRC calculation results from a previous cycle when performing a CRC calculation during a subsequent cycle.

14. The method of claim 12, wherein said step of determining comprises selecting one of the plurality of CRC modules based on a number of bytes in the current segment of data.

15. The method of claim 14, wherein if the current segment of data comprises a number of bytes, which is less than the maximum number of bytes:

said step of determining comprises selecting, from the plurality of CRC modules, a CRC module configured for performing the CRC calculation on the number of bytes in the current segment of data; and

said step of processing comprises using the selected CRC module to perform the CRC calculation on the current segment of data to produce final CRC calculation results.

16. The method of claim 14, wherein if the current segment of data comprises more than the maximum number of bytes:

said step of determining comprises selecting the at least one CRC module configured for performing the CRC calculation on the maximum number of bytes;

said step of processing comprises using the selected CRC module to perform the CRC calculation on the current segment of data to produce CRC calculation results for the current cycle; and

wherein prior to said step of repeating, said method further comprises:

storing the CRC calculation results for the current cycle; and

ascertaining if a next segment of data will be supplied to the multiple-byte CRC circuit during a next cycle, and if so, whether the next segment of data comprises more than the maximum number of bytes.

17. The method of claim 16, wherein if the method ascertains that a next segment of data is not supplied to the multiple-byte CRC circuit, the stored CRC calculation results are considered final CRC calculation results and the method ends.

18. The method of claim 16, wherein if the method ascertains that a next segment of data is supplied to the multiple-byte CRC circuit and it comprises more than the maximum number of bytes:

said step of determining comprises selecting the at least one CRC module configured for performing the CRC calculation on the maximum number of bytes;

said step of processing comprises using the selected CRC module to perform the CRC calculation on the next segment of data and the stored CRC calculation results to produce CRC calculation results for the next cycle; and

said step of storing comprises replacing the stored CRC calculation results with the CRC calculation results for the next cycle.

19. The method of claim 16, wherein if the method ascertains that a next segment of data is supplied to the multiple byte CRC circuit and it comprises a number of bytes, which is less than the maximum number of bytes:

said step of determining comprises selecting, from the plurality of CRC modules, a CRC module configured for performing the CRC calculation on the number of bytes in the next segment of data;

said step of processing comprises using the selected CRC module to perform the CRC calculation on the next segment of data and the stored CRC calculation results to produce CRC calculation results for the next cycle; and

said step of storing comprises replacing the stored CRC calculation results with the CRC calculation results for the next cycle.

20. The method of claim 16, wherein if the method ascertains that a next segment of data is supplied to the multiple byte CRC circuit and it comprises a number of bytes, which is less than the maximum number of bytes:

said step of determining comprises selecting the at least one CRC module configured for performing the CRC calculation on the minimum number of bytes;

said step of processing comprises using the selected CRC module to perform the CRC calculation on a first byte of the next segment of data and the stored CRC calculation results to produce new CRC calculation results;

said step of storing comprises replacing the stored CRC calculation results with the new CRC calculation results; and

repeating the steps of processing and storing until no bytes remain in the next segment of data.

IX. EVIDENCE APPENDIX

No evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title has been entered during the prosecution of the captioned case. In addition, no evidence has been entered by the examiner.

X. RELATED PROCEEDINGS APPENDIX

No other prior and pending appeals, interferences, or judicial proceedings are known to Appellant or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.